REMARKS

In the Office Action, claims 41-45, 47-54 and 56-57 are rejected under 35 U.S.C. §103(a) as being unpatentable over Venkateshwaran et al. in view of Rostoker et al. and further in view of Akram et al.

In response to the rejection, claims 41 and 49 are further amended to clearly define the subject matter of the invention in a patentable way to overcome the rejection under 35 U.S.C. §103(a). More specifically, the amended independent claim 41 now includes the limitation that the multi-chip package structure comprises **a multi-chip module substrate** and at least two chip packages, **each of said chip packages being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein,** said at least two chip packages having been burn-in tested and function tested. Similarly, the amended independent claim 49 includes the limitation that the multi-chip package structure comprises **a multi-chip module substrate and at least one chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein,** said at least one chip package having been burn-in tested and function tested. The amended claims 41 and 49 should be patentable because none of the prior arts cited by the Examiner has taught, disclosed or suggested the structure of **a packaged chip module within a multi-chip module package structure**.

Venkateshwaran et al. teach a stacked multi-chip assembly including a plurality of **integrated circuit die** directly attached to a substrate having pads corresponding to

terminals on the die, and interconnections between the die, and also to external contacts. On page 2 of the Office Action, the Examiner refers to the device 201 of Venkateshwaran et al. as a chip package. On page 3 of the Office Action, the Examiner refers to the same device 201 as a bare chip. Applicants like to point out that throughout the disclosure of Venkateshwaran et al., it is clearly indicated that **a die** 201 (col. 1, line 58) or **integrated dices** (col. 3, lines 63) **not a packaged chip module** are connected or bonded to a substrate.

In the amended claims 41 and 49, the multi-chip module package structure has a **multi-chip substrate**, and the chip package has **a bare chip and a chip substrate** packaged and enclosed within a packaged chip module. In comparison to the instant invention, the device 201 and the substrate 211 of Venkateshwaran et al. are a bare chip and a chip substrate respectively of a conventional chip scale package. The bare chip is connected to the chip substrate by wires or ball bumps. It is clear that the semiconductor device of Venkateshwaran et al. cited by the Examiner is a conventional chip scale package in which two bare dies are packaged. As taught by Venkateshwaran et al., the chip scale package is ready for interconnection on a printed wiring board (col. 1, lines 60-63). No where have Venkateshwaran et al. suggested that **the chip scale package with another chip scale package or a bare die can be further packaged and enclosed in a multi-chip module package structure**. Applicants respectfully contend that the structure cited by the Examiner only shows a chip scale package which is different from the multi-chip module package of the instant invention.

In the Office Action, the Examiner cited on page 2 that the substrate 211 and the bare dies 201 of Venkateshwaran et al. correspond to the (multi-chip module) substrate and the chip packages respectively of claim 41. As pointed out earlier, Venkareshwaran et al. repeatedly describe the element 201 as a bare die rather than a chip package. It is clear that the Examiner's citation that claim 41 is unpatentable over Venkateshwaran et al. is unwarranted because of the different physical structure.

Although it has been pointed out in the Remarks of AMENDMENT B, applicants like to reiterate that **a bare chip is a semiconductor die cut from a wafer**. **A bare chip or a semiconductor die is different from a packaged chip module** of this invention in that a packaged chip module is a finished chip package that comprises **a bare die on a chip substrate** embedded within the chip package, burn-in tested and function tested. **In other words, a packaged chip module is a protected module which has *a known good die* embedded therein and guaranteed to be functional but a bare chip is not protected and may be already defective.**

There are several advantages in using a packaged chip module rather than a bare chip in packaging a multi-chip module. One is that it avoids the possibility of packaging a bare chip that may not be functional at all in the first place. The other is that the packaged chip module is much better protected than a bare chip from being damaged during the multi-chip packaging process. Because a multi-chip module comprises multiple chips and is usually a high cost product, having high yield is very important in manufacturing. **None of the prior arts including those cited by the Examiner has ever taught, suggested or**

anticipated the structure of a multi-chip module having a packaged chip module therein.

As pointed out in the specification and the remarks in the response to a previous office action, the gist of this invention is to provide a multi-chip package structure that integrates at least an **already packaged and tested chip module onto the substrate of the multi-chip package structure**. By integrating a packaged chip module, the yield of the multi-chip package is greatly increased because the **packaged chip module has passed both burned-in and function test**. The unique technique of the instant invention has not been known and practiced in the industry and has provided significant improvement in high yield and benefit for manufacturing a multi-chip module.

Akram et al. teach a semiconductor package comprising multiple stacked substrates having flip chips attached to the substrates with chip on board assembly techniques to achieve dense packaging. As can be seen in the disclosure of Akram et al., a plurality of **first semiconductor dice 128 (col. 6, line 13), a plurality of second semiconductor dice 150 (col. 6, line 38), ..., or a plurality of fourth semiconductor dice 474 (col. 8, line 23), ...** rather than **a packaged chip module as claimed in claims 41 and 49** is used in the stacked substrate chip assembly. The Examiner states that Akram et al. disclose a package material enclosing a substrate, a connect point and a chip package to achieve dense packaging. Applicants respectfully contend that Akram et al. never disclose any chip packages. As pointed out earlier, **only semiconductor dice** is disclosed by Akram et al.

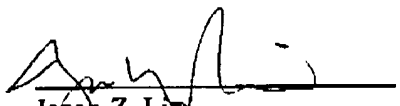
Rostoker et al. disclose a technique for individually testing unsingulated dies on a wafer. Conductive lines extend on the wafer from electronic mechanisms for selecting dies to the individual dies. The teaching of Rostoker et al. is to facilitate burn-in and functional test of dies at wafer level. Because the subject matter of Rostoker et al. is different from the instant invention, **it has never disclosed or suggested packaging a chip package in a multi-chip module package structure**. Neither do Venkateshwaran et al. teach the multi-chip module package structure of the present invention. It is not logical for a person with ordinary skill in the art to modify Venkateshwaran et al. to reach the instant invention.

None of the cited prior arts has taught or suggested **packaging an already packaged chip module which has a bare die and a chip substrate, and has been burn-in tested and function tested to form a multi-chip package structure**. Therefore, a person having ordinary skill in the art can not reach the subject matter of the invention even if all the cited prior arts are combined.

From the foregoing discussion, it is clear that the instant invention differs from the cited prior arts. The physical difference results in different effects and is not obvious. A paragraph is added in the specification in the above amendment to clearly describe the subject matter of the invention. The amended base claims 41 and 49 have clearly defined the unique feature of this invention and overcome all rejection 35 U.S.C. §103(a) and should be patentable. By virtue of dependency, claims 42-45, 47-48 and 50-54, 56-57 should also be patentable.

It appears to the applicants that the Examiner made the rejection without considering the arguments that applicants made in the Remarks of AMENDMENT B regarding the fact that Venkateshwaran et al. only teach **packaging bare dies in a conventional chip scale package** instead of packaging conventional chip scale packages in a multi-chip module package. Applicants respectfully request that the Examiner reconsider the amended claims along with the above remarks. Prompt and favorable reconsideration of the application is respectfully solicited.

Respectfully submitted,



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Version with Markings to Show Changes Made

CLAIMS:

41. (Twice Amended) A multi-chip module package structure comprising:

a multi-chip module substrate;

at least two chip packages, each of said chip packages being a packaged chip module having a bare chip and a chip substrate packaged and [embedded] enclosed therein, said at least two chip packages having been burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said chip packages with said multi-chip module substrate;

a plurality of electrical connect pins; and

a package material enclosing said multi-chip module substrate, said connect points and said chip packages.

49. (Twice Amended) A multi-chip module package structure comprising:

a multi-chip module substrate;

at least a bare chip;

at least one chip package[, said chip package] being a packaged chip module having a bare chip and a chip substrate packaged and [embedded] enclosed therein, said at least one chip package having been burn-in tested and function tested;

a plurality of electrical connect points electrically connecting said bare chip and said at least one chip package with said multi-chip module substrate;

a plurality of electrical connect pins; and

a package material enclosing said multi-chip module substrate, said connect points, said bare chip and said at least one chip package.